IN THE CLAIMS:

Please amend the claims as follows:

Listing of Claims:

1. (Previously Presented) An integrated processor system comprising:

a common integrated circuit substrate holding each of:

(1) a processing unit for performing arithmetic and logical operations;

(2) at least one internal system storage structure selected from the group consisting of caches, buffers, and registers;

(3) an external memory interface for connecting to an external memory not on the common substrate;

wherein the processing unit executes at least a portion of a bootstrap program to select between different external memory set-up data needed to communicate with different types of external memory while using the at least one internal system storage structure for temporary storage without access to external memory.

2. (Original) The integrated processor system of claim 1 further including: interface circuits for communicating electrical signals with non-memory external devices.

3. (Original) The integrated processor system of claim 1 further including: a memory interface for communicating with external memory; and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of external memory setup data required for the memory interface to initiate communication with external memory.

4. (Original) The integrated processor system of claim 3 further including: a network interface and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data through a network connection.

5. (Original) The integrated processor system of claim 3 wherein the external memory

includes non-volatile memory and volatile memory and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data for the external volatile memory from the external non-volatile memory.

6. (Original) The integrated processor system of claim 1 comprising wherein the external non-volatile memory is flash memory.

7. (Original) The integrated processor system of claim 3 wherein the processing unit includes an address translation table mapping processing unit addresses to addresses of the external memory and wherein the processing unit executes at least a portion of the bootstrap program to make a temporary address translation table in a buffer memory so as to make the cache memory available for temporary storage.

8. (Original) The integrated processor system of claim 1 wherein the system storage structure is a cache memory and wherein the processing unit executes at least a portion of the bootstrap program to read arbitrary data into the cache memory and then to lock the cache memory against further reading or writing to external memory so that it may be used as variable storage for further execution of the bootstrap program.

9. (Original) The integrated processor system of claim 3 wherein the processing unit further executes at least a portion of the bootstrap program to store the memory setup data in the memory interface and further load additional programs for execution into external memory.

10. (Original) The integrated processor system of claim 3 wherein the processing unit further executes at least a portion of the bootstrap program to store the memory setup data in the memory interface and then to execute a program contained in external memory.

11. (Original) The integrated processor system of claim 3 wherein the memory setup data is selected from the group consisting of: memory type as static or dynamic, memory speed, memory size, memory parity, and memory timing.

12. (Previously Presented) A method of initializing an integrated processor system including, on a common integrated circuit substrate, a processing unit for performing arithmetic and logical operations; at least one internal system storage structure selected from the group consisting of: caches, buffers, and registers; and an external memory interface for connecting to an external memory not on the common substrate comprising the step of:

executing at least a portion of a bootstrap program by the processing unit to select between different external memory set-up data needed to communicate with different types of external memory while using the at least one internal system storage structure for temporary storage without access to external memory.

13. (Original) The method of initializing an integrated processor system of claim 12 wherein the processor system further includes interface circuits for communicating electrical signals with non-memory external devices.

14. (Original) The method of initializing an integrated processor system of claim 12 wherein the processor system further includes a memory interface for communicating with external memory; and

including the step of executing at least a portion of the bootstrap program by the processing unit to provide for the acquisition of external memory setup data required for the memory interface to initiate communication with external memory.

15. (Original) The method of initializing an integrated processor system of claim 14 wherein the processing unit further includes a network interface and including the step of executing at least a portion of the bootstrap program by the processing unit to provide for the acquisition of the external memory setup data through a network connection.

16. (Original) The method of initializing an integrated processor system of claim 14 wherein the external memory includes non-volatile memory and volatile memory and including the step of executing at least a portion of the bootstrap program by the processing unit to provide for the acquisition of the external memory setup data for the external volatile memory from the external non-volatile memory.

17. (Original) The method of initializing an integrated processor system of claim 14 wherein the processing unit includes an address translation table mapping processing unit addresses to addresses of the external memory and including the step of executing at least a portion of the bootstrap program to make a temporary address translation table in a buffer memory so as to make the cache memory available for temporary storage.

18. (Original) The method of initializing an integrated processor system of claim 12 wherein the system storage structure is a cache memory and including the step of executing at least a portion of the bootstrap program by the processing unit to read arbitrary data into the cache memory and then to lock the cache memory against further reading or writing to external memory so that it may be used as variable storage for further execution of the bootstrap program.

19. (Original) The method of initializing an integrated processor system of claim 14 including the step of executing at least a portion of the bootstrap program by the processing unit to store the memory setup data in the memory interface and further load additional programs for execution into external memory.

20. (Original) The method of initializing an integrated processor system of claim 14 including the step of executing at least a portion of the bootstrap program by the processing unit to store the memory setup data in the memory interface and then to execute a program contained in external memory.

21. (Original) The method of initializing an integrated processor system of claim 14 wherein the memory setup data is selected from the group consisting of: memory type as static or dynamic, memory speed, memory size, memory parity, and memory timing.

22. (Previously Presented) The method of initializing an integrated processor system of claim 12 wherein the bootstrap program is stored in a bootstrap memory also on the common integrated circuit substrate.

23. (Previously Presented) The integrated processor system of claim 1 wherein the bootstrap program is stored in a bootstrap memory also on the common integrated circuit substrate.